

**Claims**

What is claimed is:

5 1. A circuit, comprising:

a first operation unit operably coupled to receive a first set of operands, wherein  
the first operation unit combines the first set of operands to produce a first operation  
result, wherein subsequent to receipt of the first set of operands, the first operation unit  
10 receives a second set of operands and combines the second set of operands to produce a  
second operation result;

15 a pre-accumulation register operably coupled to the first operation unit, wherein  
the pre-accumulation register stores the first operation result to produce a buffered first  
operation result;

20 a second operation unit operably coupled to receive a third set of operands,  
wherein the second operation unit combines the third set of operands to produce a third  
operation result, wherein a first operand of the third set of operands is the second  
operation result;

memory operably coupled to the second operation unit, wherein the memory  
stores the third operation result in one of a plurality of memory locations; and

25 a selection block operably coupled to the memory, the second operation unit, the  
pre-accumulation register, and the first operation unit, wherein the selection block selects  
a second operand of the third set of operands from a set of potential operands, wherein  
the set of potential operands includes the second operation result, the buffered first  
operation result stored in the pre-accumulation register, and data stored in at least one of  
30 the plurality of memory locations of the memory, wherein the selection block selects the

second operand of the third set of operands based on operand selection information included in an operational code received by the circuit.

5 2. The circuit of claim 1, wherein the selection block is operably coupled to receive at least one additional operand, wherein the at least one additional operand is included in the set of potential operands.

10 3. The circuit of claim 1 further comprises accumulation buffer operably coupled to the second operation unit and the selection block, wherein the accumulation buffer stores the third operation result to produce a buffered third operation result, wherein the buffered third operation result is included in the set of potential operands.

15 4. The circuit of claim 1, wherein the first operation unit is a multiplier.

5. The circuit of claim 4, wherein the second operation unit is an adder.

## 6. A circuit, comprising:

a first operation unit operably coupled to receive a first set of operands, wherein the first operation unit combines the first set of operands to produce a first operation result, wherein subsequent to receipt of the first set of operands, the first operation unit receives a second set of operands and combines the second set of operands to produce a second operation result;

10 a plurality of pre-accumulation registers operably coupled to the first operation unit, wherein each pre-accumulation register of the plurality of pre-accumulation registers corresponds to a different thread of a plurality of threads,

15 wherein when the first operation result produced by the first operation unit is a result of an operation for a selected thread of the plurality of threads, a pre-accumulation register that corresponds to the selected thread stores the first operation result to produce a buffered first operation result corresponding to the selected thread;

20 a second operation unit operably coupled to receive a third set of operands, wherein the second operation unit combines the third set of operands to produce a third operation result, wherein a first operand of the third set of operands is the second operation result;

memory operably coupled to the second operation unit, wherein the memory stores the third operation result in one of a plurality of memory locations; and

25 a selection block operably coupled to the memory, the second operation unit, the plurality of pre-accumulation registers, and the first operation unit, wherein the selection block selects a second operand of the third set of operands from a set of potential operands, wherein the set of potential operands includes the second operation result, the buffered first operation result stored in the plurality of pre-accumulation registers, additional buffered results stored in the plurality of pre-accumulation registers, and data stored in at least one of the plurality of memory locations of the memory, wherein the

selection block selects the second operand of the third set of operands based on operand selection information included in an operational code received by the circuit.

7. The circuit of claim 6, wherein the selection block is operably coupled to receive  
5 at least one additional operand, wherein the at least one additional operand is included in  
the set of potential operands.

8. The circuit of claim 6 further comprises an accumulation buffer operably coupled  
to the second operation unit and the selection block, wherein the accumulation buffer  
10 stores the third operation result to produce a buffered third operation result, wherein the  
buffered third operation result is included in the set of potential operands.

9. The circuit of claim 6, wherein the first operation unit is a multiplier.

15 10. The circuit of claim 9, wherein the second operation unit is an adder.

11. The circuit of claim 6, wherein the first operation unit receives a fourth set of  
operands, wherein the first operation unit combines the fourth set of operands to produce  
a fourth operation result, wherein the first operation unit combines the fourth set of  
20 operands subsequent to combining the first set of operands and prior to combining the  
second set of operands.

12. A method for executing operation codes in a computation block, comprising:

receiving a first set of operands during a first cycle;

5 combining the first set of operands using a first operation unit during the first cycle to produce a first operation result;

storing the first operation result in a pre-accumulation buffer during a second cycle to produce a buffered first operation result;

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receiving a second set of operands during the second cycle;

15 combining the second set of operands using the first operation unit during the second cycle to produce a second operation result;

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selecting a first operand of a third set of operands from a set of potential operands that includes the buffered first operation result, wherein selecting the first operand of the third set of operands occurs during a third cycle, wherein selecting the first operand of the third set of operands is based on a current operation code; and

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combining the second operation result and the buffered first operation result using a second operation unit during the third cycle to produce a third operation result.

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13. The method of claim 12 further comprises storing the third operation result in a memory during a fourth cycle, wherein the set of potential operands includes previously determined operation results stored in the memory.

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14. The method of claim 12, wherein storing the first operation result further comprises storing the first operation result in a pre-accumulation buffer of a plurality of pre-accumulation buffers, wherein the pre-accumulation buffer is selected based on a thread of a plurality of threads to which the current operation code corresponds, wherein

the set of potential operands includes previously buffered results stored in each of the plurality of pre-accumulation buffers.